DASSAULT SYSTEMES

ENOVIA

SOFTWARE AND SYSTEM-ON-A-CHIP DESIGNER

OBJECTIVE

Software and System-on-a-Chip Designer enables collaboration on software and semiconductor designs to effectively manage changes coming from multiple contributors from within the enterprise. Data can be managed at both the detailed file/directory level, and at a "modular" level of abstraction. Design data contributed by individual teams can be seamlessly integrated into higher level designs.

OVERVIEW

Software and System-on-a-Chip Designer leverages a unique modular approach to Design Data Management which is optimized for efficient design reuse and multisite collaboration. IP blocks managed as modules are hierarchically combined into designs which are correct-by-construction. Data is managed at the file level within a module, and at the modular level of abstraction as hierarchical connections between modules. As the design changes, new data is automatically replicated at each design site in module and file caches and shared across workspaces. This data sharing infrastructure maximizes performance and guarantees the most efficient use of disk space which can be especially important for large hardware and software designs, Design tool configuration settings and customizations can also be shared across design sites guaranteeing that all design work is performed in a controlled design environment. Hierarchical data structures can be replicated and automatically synchronized as changes occur with Hierarchical Product Structures in **3D**EXPERIENCE®, providing a tight integration with enterprise applications such a Hierarchical Defect Tracking and enterprise wide IP management.

HIGHLIGHTS

High Performance

The most important capability for a Design Data Management tool is performance. Designers cannot afford to wait for workspaces to be updated with changes coming from a distributed team. Today's large System-On-A-Chip designs can be composed to hundreds of individual IP blocks contributed by multiple design teams. Because most data needed in a workspace to view, netlist, simulate, etc. is not being modified by an individual designer, cached read-only data is shared across workspaces as efficiently as possible by creating symlinks to locally cached IP blocks in module caches, and hardlinks to file versions in file caches.

Caches are automatically updated as changes occur so that data is locally available before it is needed in a workspace. Data is only physically copied into a workspace when it needs to be edited. A workspace for a terabyte design properly partitioned into individual modules for IP blocks can be populated in seconds. Data transfer speed is also maximized.

Design IP blocks can be managed in modules distributed across multiple servers, allowing for local performance optimization by co-locating repository servers and development teams, and eliminating a single point of failure. A hierarchical design does not exist in its entirety and any single server. Rather, modules included in a hierarchical design are fetched from the servers in which they are managed, and assembled in single directory structure in a workspace, leveraging the caching mechanisms to efficiently share read-only data. Change set processing provides for efficient workspace updates, and delta transfers can be enabled when appropriate to maximize data transfer efficiency.

Simple Multisite Administration - Leverage Administrative Expertise Across Design Sites

Administration of the sophisticated infrastructure required at each design site to support efficient workspace creation and update is greatly simplified using Enterprise Development Administration, eliminating the need for deep administrative expertise at each site. A server is setup at each design site and configured to manage all of the client-side infrastructure associated with supporting a set of workspaces for each development project at the site. The server automatically replicates design data as it changes in module and file caches, and automates cache maintenance, removing data as it is no longer needed. In a multisite environment it is not enough to guarantee that the right data is being shared. It is also critical that design tools used to modify data are correctly configured when launched. To join a project, a designer chooses from a list of developments being managed by the local server, creates a workspace, and then launches one or more tools work with the data. If a designer changes from working on one project to another, the design environment changes accordingly. A design tool configuration module for each development is automatically replicated across all sites, enabling centralized administration of the design environment. Template configuration modules encapsulating best-practice tool settings for Analog, Digital, and Software design methodologies are provided, enabling rapid deployment.

Tight Integration between Work-In-Process and Enterprise Level Activities

Activity associated with complex system designs, whether for hardware or software, occurs at both the Work-in-Process level and at the Enterprise level. Work-in-Process is performed in compute environments local to design centers and may be considered as being "Below-the-Line", to distinguish it from activity which is centrally managed in an Enterprise Platform "Above-the-Line", such as Requirements Management, Project Management, IP Management, and Defect Tracking. While Work-in-Process requires detailed tracking of all changes made during the development process, only specific "releases" of IP blocks are included in hierarchical design structures which comprise higher-level products. A tight integration between the systems which manage data "Below-the-Line" and "Above-the-Line" provides for a synchronous connection between hierarchically connected product objects in the Enterprise System and actual design data managed in globally distributed DDM servers. Enterprise level collaboration is achieved by federating and synchronizing important data released by individual design teams without disrupting local design methodologies. A design hierarchy can be "pushed" from the WIP design environment to the **3D**EXPERIENCE platform. The critical design data set is extracted and product structures are created for appropriate defect tracking with **Defect Engineer**.

Protecting Sensitive IP

Some IP is so sensitive that it should never even be replicated in either module caches or file caches, which allow read-only data to be efficiently shared across multiple workspaces. The mere presence of the data in such a widely accessible disk location introduces a security concern. As such, the ability to replicate a sensitive data set to cache directories can be disabled. The only way the data can be populated is as a physical copy into a workspace for which the owner is given permission by the access control system.

Highly Configurable and Customizable

Software and System-on-a-Chip Designer is highly configurable and customizable using both command-line and graphical administration tools for managing tool configuration settings, a TCL interface and triggering system on both the client and server sides, a sophisticated Access Control System, and a C-API.

Key Benefits:

- Connect and manage your entire design chain with a unified Design Data Management system.
- Reduce time-to-market by increasing collaboration efficiency for a rapid payback and strong ROI.
- Maximize your ability to reuse existing designs and embedded software.
- Manage your design hierarchy as part of the design process.
- Utilize an intuitive built-in Submit, Integrate, Test, and Release (SITaR) workflow.
- Manage complex data types from a variety of EDA tool vendors.
- Manage software projects using the Microsoft Visual Studio and Eclipse plug-ins.

Integrated with the Tools Designers Already Use

Besides the standard command line and GUI interfaces, **Software and System-on-a-Chip Designer** is integrated with popular EDA (Electronic Design Automation) tools for hardware design and IDEs (Integrated Development Environments) for software design. "Connectors" are available for:

Hardware Design

- Cadence® Virtuoso (Graphical schematic capture and layout)
- Synopsys® Custom Designer (Graphical schematic capture and layout)
- Synopsys Galaxy Platform (Automated Place & Route)

Software Design

- Eclipse IDE
- Microsoft Visual Studio IDE

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