SILICON THINKING INDUSTRY SOLUTION EXPERIENCE

SEMICONDUCTOR DESIGN DATA MANAGEMENT
Advancements in integrated circuit (IC) density and competition for market leadership drive demand for more complex devices from semiconductor manufacturers. To compete successfully, manufacturers must use teams of diverse design specialists and complex project workflows to maximize device differentiation and team productivity. As a result, IC projects carry increasing business risk.

Dassault Systèmes Silicon Thinking Industry Solution Experience powered by the 3DEXPERIENCE® platform provides a portfolio of IC design and engineering performance enhancements that help mitigate project risk, shorten time-to-market, and increase product quality and yield. Silicon Thinking provides these benefits through:

- Efficient intellectual property (IP) management and reuse
- Graphical analytics to manage design closure
- Instant access to the latest design data for all design teams
- End-to-end traceability, from requirements to verification and validation
- Packaging reliability simulation and testing
- Enhanced product variation and defect management

With this solution portfolio, semiconductor manufacturers can more quickly and easily untangle the simultaneous challenges they face from the demands of increasing chip complexity, lowering power consumption, and achieving faster time-to-production and higher yields.
SEMICONDUCTOR COLLABORATIVE DESIGN PROCESS

Enable collaborative design for complex semiconductor projects

Dassault Systèmes Silicon Thinking Semiconductor Collaborative Design process integrates design data management from ENOVIA Synchronicity® DesignSync® and deep design analytics from ENOVIA® Pinpoint® to enhance team productivity for IC design. This process experience is used today by over 120 IC development organizations around the world to boost design team productivity.

**ENOVIA Synchronicity DesignSync**

ENOVIA Synchronicity DesignSync helps centralize IC design data management for large, distributed projects. Design data is captured directly from electronic design automation (EDA) tools into a hierarchical data structure, which then provides coordinated access for distributed design teams. This hierarchical structure directly supports an IP-block assembly approach for rapidly designing customer-specific ICs. It helps simplify and speed integration of design sub-elements into the overall IC design, facilitating design reuse.

**ENOVIA Pinpoint**

ENOVIA Pinpoint provides managers with dashboards and graphical analytics to assess and accelerate design closure. ENOVIA Pinpoint enables analysis of diverse design, simulation, and testing data with historical timelines to help you see where projects might be diverging from planned milestones. Project managers and designers have a shared view from which to make joint project management decisions.

**Semiconductor Collaborative Design Process**

To help ensure that complex integrated designs succeed, the right foundation for collaborative design and information systems is essential. Dassault Systèmes Silicon Thinking Semiconductor Collaborative Design process:

- Scales across large, distributed teams
- Supports IP reuse and variant optimization
- Works with multiple application platforms and keeps designers “designing”
- Maximizes information access
- Accelerates project decision making through automated, advanced analytics and dashboards

13 of the top 15 semiconductor companies around the world are using Dassault Systèmes Silicon Thinking Collaborative Design to boost design productivity.
Advanced design data management for complex IC projects. ENOVIA Synchronicity DesignSync is an end-to-end semiconductor design data management system. It simplifies and accelerates IP block development and reuse, with IP block integration simplified, data sharing accelerated, and any design flaws more easily identified and managed. Integration engineers can support more complex designs with more IP blocks without needing additional resources.
Compartmentalizing in the electronics market requires constant, unending functionality enhancements. Outsourcing of design work, inbound licensing of IP, variant reuse, and distributed development teams are all necessary to achieve the required functionality levels at an acceptable cost to compete in today’s electronics markets.

**MULTIPLE CONFLICTING CHALLENGES MUST BE OVERCOME:**

1. Use of different design data systems by the various design teams to suit their specific design data capture needs.
2. Flaws unknowingly reintroduced by incorrect selection of design branch variants.
3. Extremely high rates of change for individual components making the maintenance of a consistent integration at the chip level very difficult and time-consuming.
4. IC designs include ever-increasing amounts of embedded software, each of which can be an area of specialization, with unique design specifications and data.

**CAUSES OF THESE CHALLENGES:**

1. Business demand for ever more complex ICs, especially the current demand for systems on chips (SoCs), forces independent device manufacturers (IDMs) and fabless manufacturers to have ever more complex design organizations and processes.
2. Diversification of IC design specialties for processors, memory, display management, power, radio frequency (RF) connectivity, security, and sensor control now drive use of diverse design tools and data.
3. Specialist teams choose design data management systems that are best suited to their area of expertise, with less consideration for design data integration with other teams.

**WHAT CAUSES THESE ISSUES AND PAIN POINTS?**

1. The primary causes of delay and diminished product quality are the counteracting combination of IC project complexity, low efficiency design, testing, and limited results analysis tools.
2. Ineffective communication between engineers and teams impedes timely and high-quality design completion. Communication can be inhibited by geographic location, time zones, spoken language, culture, skill set, and process knowledge.
3. Limited budget for design tool licenses needed for collaborative analysis.
FINDING THE RIGHT DESIGN DATA MANAGER FOR YOUR IC PROJECTS

An ideal IC design project would be delivered on time and on budget, while meeting requirements for functionality, performance, and quality. Achieving this ideal requires a design data management process that can:

- **Efficiently incorporate design changes** through a centralized application accessible by any geographically distributed design team
- **Eliminate duplication** with a hierarchical data management system that allows reuse of unchanging core elements alongside development or modification of new elements
- **Reduce version tracking errors** through comprehensive and adaptable version and configuration controls, with modular data structures to eliminate excessive low-level file diffs
- **Include surface data needed for correct design vs. license choices** with analytics that provide interactive, drill-to-detail dashboards including both summary key performance indicators (KPIs) for at-a-glance status checking and root-cause analysis for management-by-exception
- **Accommodate any device complexity** through simplified change impact analysis and reporting, enabling more agile design activity decision making
- **Enable any team organization complexity** using broad and adaptable version and configuration controls
- **Permit all design tool data output** through modular data structures and hierarchical data management that allows reuse of unchanging core elements alongside development or modification of new elements

It is exactly these capabilities that are provided by the ENOVIA Synchronicity DesignSync application.
ACCELERATE COMPLEX IP DESIGN PROJECTS

Key capabilities that will help differentiate your project

Throughout the design process, ENOVIA Synchronicity DesignSync organizes design data to streamline and accelerate integration. In fact, this advantage makes DesignSync a data design manager of choice for 13 of the top 15 semiconductor companies. Its flexible architecture works to provide both up-to-date data across all design team sites and minimal replication and update data flow. DesignSync provides end-to-end design chain data management for both hardware and software designs. It provides a single source of truth (SSoT) for your entire work-in-progress IP portfolio.

Encapsulating IP block development into module hierarchies aligns directly with commonly structured design projects using geographically distributed teams, making design data integration simple and streamlined. Teams can create multiple levels of hierarchical project content. Data structures can be configured to support multiple design methodologies and security models, while also enforcing best practices.

DesignSync provides support for extremely large sets of complex (ASCII and binary), composite (multiple files across directories to create a single design object) and EDA-tool proprietary data types. Integration into multiple development tools (including Cadence® DFI, Synopsys® Custom Design and Galaxy, Eclipse IDE, and Microsoft® Visual Studio®, along with a stand-alone graphical user interface (GUI), command line access, a Tcl shell, and application programming interface (APIs)) help streamline data management and maximize user adoption.

DesignSync also interoperates with other ENOVIA products and integrates to legacy systems and tools to provide a complete enterprise-PLM solution.
DESIGNSYNC ARCHITECTURAL ADVANTAGES

Unique system capabilities that can dramatically advance your design data management

<table>
<thead>
<tr>
<th>Feature</th>
<th>Advantage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Modules, files, hierarchical configuration managers (HCMs) can all be part of a DesignSync project database</td>
<td>Migration from file-based to module-based data management can be evolutionary</td>
</tr>
<tr>
<td>Project files can be organized into a hierarchy of modules</td>
<td>Simplifies version diffs, leading to dramatically faster workspace opens, fewer version errors, better product quality</td>
</tr>
<tr>
<td>Reference or replicate files from other data management systems, such as Perforce™ or Rational®</td>
<td>Allows a single source of truth for your entire project</td>
</tr>
<tr>
<td>Centralized version management</td>
<td>Assures one version of truth for all project designers</td>
</tr>
<tr>
<td>Modular change set processing – new vs. existing version comparisons done at the set level, not file level</td>
<td>Designer workspace open and initialization 2x to 100x faster</td>
</tr>
<tr>
<td>Distributed Design Hierarchies – Design hierarchy element managed locally, but available globally</td>
<td>Mirrors real-world structure of design teams and SoC IP. Optimized for fastest possible opens and check-outs by designers</td>
</tr>
<tr>
<td>Real-time asynchronous distributed cache updates – predictive replication</td>
<td>System automatically updates all local caches when new design module versions checked-in. Dramatically faster workspace opens/check-outs</td>
</tr>
<tr>
<td>128-bit SSL encryption</td>
<td>Secure file transfers help prevent piracy during data replication</td>
</tr>
</tbody>
</table>

DesignSync is built on a unique highly scalable client/server architecture capable of terabyte data management with millions of large GB-scale files. Static, dynamic, and hierarchical file use models are supported. Configurable desktop and group server caching allows fast opens for read-only data which comprises the majority of workspace data. Deployed systems can include multi-level mirror servers to optimize the conflicting demands of workspace access speed and update distribution speed. IC project data can be distributed physically across multiple repositories co-located with their design teams, but managed centrally so that every team has the same single version of truth.
DESIGNSYNC ARCHITECTURAL ADVANTAGES

Unique user interface capabilities that will dramatically advance your design data management

<table>
<thead>
<tr>
<th>Feature</th>
<th>Advantage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Where-used analytics</td>
<td>Lists easily generated for design elements with faults or other key attribute</td>
</tr>
<tr>
<td>Embedded into leading EDA and software development tools (Cadence, Synopsys, Mentor Graphics®, Microsoft, and others)</td>
<td>Users manage files from within the design application, streamlining data file read/write and check-in/check-out</td>
</tr>
<tr>
<td>Built-in two- and three-way file comparisons for ASCII files, such as register transfer level (RTL)</td>
<td>Accelerates version management and fault location</td>
</tr>
<tr>
<td>Graphical and command line user interfaces (UIs)</td>
<td>Adapts to user-preferred UI</td>
</tr>
</tbody>
</table>

Identify where design elements are used

DesignSync access from within leading EDA and software development tools

Compare differences between 2 or 3 files
Since 1998, IC design teams have relied on ENOVIA Synchronicity, in particular ENOVIA Synchronicity DesignSync, to help manage hardware and software data in their products. Today, over 120 semiconductor development organizations take advantage of ENOVIA Synchronicity to boost design productivity. ENOVIA Synchronicity was designed specifically for design data management (DDM) of complex IC design, and continues to evolve as challenges facing the semiconductor industry evolve as well.

### Key Benefits

<table>
<thead>
<tr>
<th>Design Engineering Time Saved</th>
<th>Average % Improvement</th>
</tr>
</thead>
<tbody>
<tr>
<td>Time saved looking for correct data – Finding actual tapeout,</td>
<td>41%</td>
</tr>
<tr>
<td>rework, verified data, etc.</td>
<td></td>
</tr>
<tr>
<td>Time saved recreating mishandled data – Redesign or rollback</td>
<td>69%</td>
</tr>
<tr>
<td>time because of lost or damaged data</td>
<td></td>
</tr>
<tr>
<td>Time saved simulating wrong data – Simulating incorrect or</td>
<td>49%</td>
</tr>
<tr>
<td>changed data and libraries</td>
<td></td>
</tr>
<tr>
<td>Time saved laying out wrong data – Laying out with incorrect</td>
<td>59%</td>
</tr>
<tr>
<td>or changed components</td>
<td></td>
</tr>
<tr>
<td>Time saved verifying data – Verifying incorrect or changed</td>
<td>53%</td>
</tr>
<tr>
<td>layouts</td>
<td></td>
</tr>
<tr>
<td>Time saved coordinating with remote sites</td>
<td>43%</td>
</tr>
<tr>
<td>Time saved to assemble IP at tapeout</td>
<td>11%</td>
</tr>
</tbody>
</table>
WHAT OUR CUSTOMERS ARE SAYING

Our publishing platform, which is based upon DesignSync, saves us two weeks of NPI cycle time on average, which in our business is substantial. We can load design workspaces in minutes that without DesignSync would take hours. While this was important with smaller projects, it is now critical for our larger ones.

— Avery De Marr, PLM Systems IT Manager, FreeScale Semiconductor

Learn how ENOVIA Pinpoint and Dassault Systèmes Silicon Thinking Industry Solution Experience can fit into your IC design process.

Contact Sales for a custom evaluation and more information about the following:

- Project & Portfolio Management
- Requirement, Traceability & Test
- Issue, Defect & Change Management
- Semiconductor Collaboration Design
- Semiconductor Package Simulation
Our 3DEXPERIENCE platform powers our brand applications, serving 12 industries, and provides a rich portfolio of industry solution experiences.

Dassault Systèmes, the 3DEXPERIENCE® Company, provides business and people with virtual universes to imagine sustainable innovations. Its world-leading solutions transform the way products are designed, produced, and supported. Dassault Systèmes’ collaborative solutions foster social innovation, expanding possibilities for the virtual world to improve the real world. The group brings value to over 170,000 customers of all sizes in all industries in more than 140 countries. For more information, visit www.3ds.com