

# DESIGN OPTIMIZATION & SENSITIVITY ANALYSIS OF PHOTONIC INTEGRATED CIRCUITS WHITEPAPER

## INTRODUCTION TO PHOTONIC INTEGRATED CIRCUITS (PICs)

Photonic technologies offer a number of attractive possibilities, such as low-loss signal transmission (e.g., in an optical fiber) or resonators with high  $Q$  values (e.g., Fabry-Perot interferometer). Photonic devices are generally also more robust to electromagnetic interference which is becoming more and more of an issue in electronics as frequencies increase. <sup>[1]</sup>

In order to employ these advantages for devices like computers, medical devices, or mobile communication devices, these photonic components need to be miniaturized similar to transistors in an electronic integrated circuit (IC). The result is referred to as a photonic integrated circuit, or PIC.

Significant progress has been made over the past years in creating integrated versions of optical components, such as waveguides, resonators, modulators, or filters. With feature sizes on the nm and  $\mu\text{m}$  scales for those components, one can create PICs on the mm scale. This enables electronic and photonic ICs to be combined, either as a hybrid on the same die, or by including both technologies in the same package.

Most recently, this has led to the availability of high-speed optical transceivers, which can operate very efficiently in a small footprint. PICs are predicted to grow briskly in the communication technologies, fueled by the ever-increasing need for bandwidth. Other markets, such as medical devices or sensors, are benefiting from the progress made on this first growth phase and development is well underway.

## DESIGN APPROACH

The design approach is in principle similar to the approach for electronic ICs, with an electromagnetic (EM) simulation tool to characterize components, a circuit simulator to simulate the overall circuit behavior, and a layout tool to create the layout for fabrication. However, there are also substantial differences, stemming from the physics. Crucially, photonic components are larger than the wavelength of the light in them, meaning that full-wave EM simulations are necessary. Similar differences exist for circuit design and layout tools: a change in the PIC layout typically directly changes the circuit behavior. Therefore, instead of treating circuit design and layout separately, it is necessary for PICs to address them together. This is commonly referred to as layout-aware circuit design.

## VPI DESIGN SUITE AND CST STUDIO SUITE.

VPI Design Suite and more specifically VPIcomponentMaker Photonic Circuits provides a focused modeling and simulation environment for experts in PIC design. It provides advanced device libraries integrated with a scalable time-and-frequency-domain simulation framework for fast and accurate modeling of complex large-scale structures comprising a mixture of hundreds of photonic, optoelectronic and electrical elements<sup>[2]</sup>.

CST Studio Suite® is a full-wave electromagnetic and photonic simulation tool. It includes a number of high-performance solvers, including FIT/FDTD, FEM and MoM. It also includes multi-physics solvers, for example to carry out opto-thermal device analysis.<sup>[3]</sup>

While not specifically addressed in this paper, it is assumed that a layout tool is also employed at the same time. VPI Design Suite offers different options to connect to such tools, for example IPKISS by Luceda Photonics.<sup>[4]</sup>

A common challenge when working with multiple tools offered by separate parties is the effort it takes to transfer data from one tool to the next. It is often left to the user to identify which data are needed and in which format. VPI Design Suite and CST Studio Suite feature a link that automatically handles the flow of data for the user. This link enables VPI Design Suite to read and modify parameters of a given CST Studio Suite model and to automatically retrieve reflection and transmission properties of the component, including all necessary data format conversions. The full-wave simulation results of the component can be pre-calculated to generate a lookup table, or the simulation can be triggered on demand by VPI Design Suite.

For more efficient workflows that involve optimization, VPI Design Suite is able to generate interpolated reflection and transmission properties between calculated data points, instead of triggering a full 3D simulation for every parameter combination. It should be noted that such interpolations can lead to non-passive or non-causal reflection and transmission properties. Correctional steps can be taken, for example by employing the macromodeling tool IdEM<sup>[5]</sup> for advanced model-fitting to the interpolated data. A detailed discussion of this aspect is beyond the scope of this paper and for simplicity we will assume that the interpolated reflection and transmission properties used in this work were either corrected or sufficiently passive and causal to begin with.

## DESIGN AND FABRICATION CHALLENGES

Designing an ideal circuit that carries out a specific purpose is a first step, but more effort is needed to create a design that can work after fabrication. The main reason for this is fabrication tolerances. Fabrication tolerances lead to both systematic and random deviations of the circuit properties.

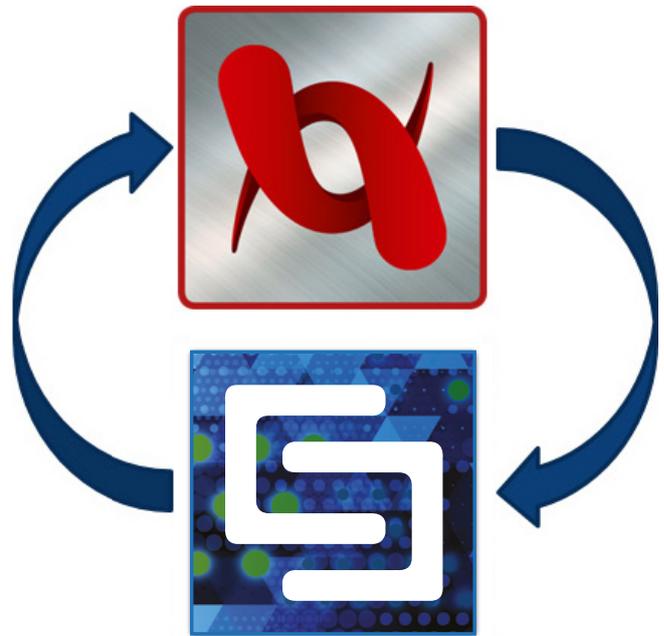


Figure 1: Automated link between VPI Design Suite and CST Studio Suite.

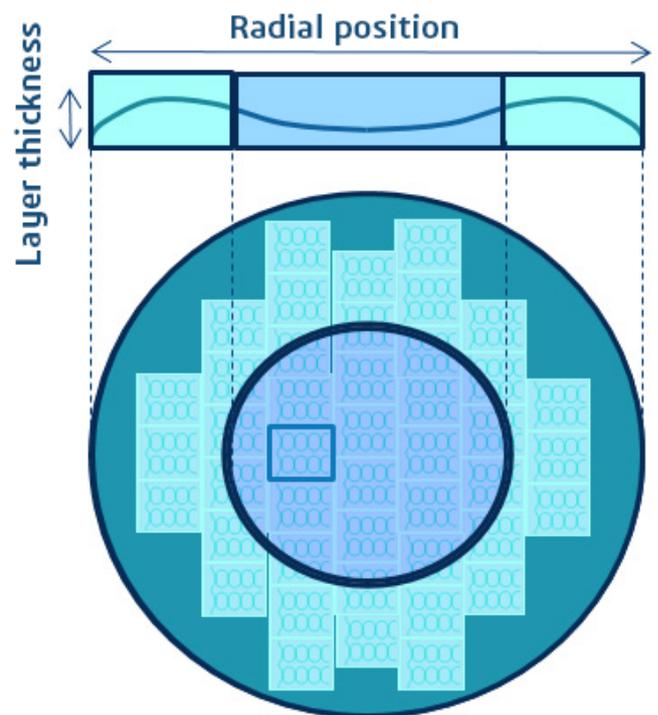


Figure 2: Large scale fabrication variations.

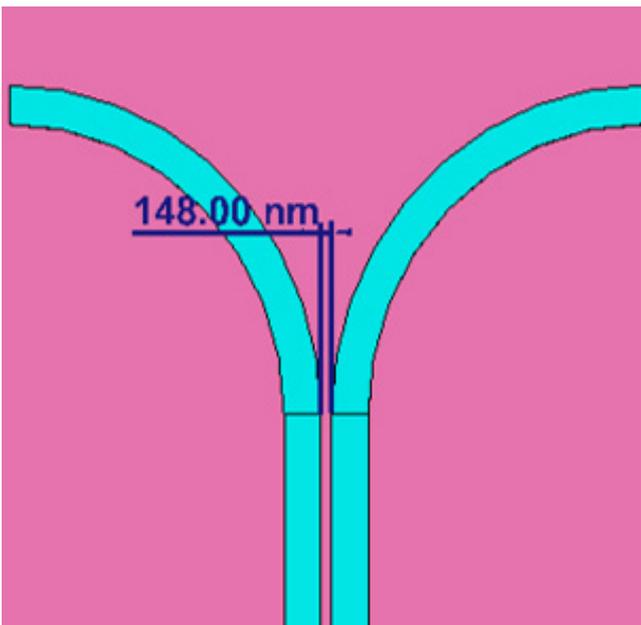
In general, one can distinguish three different classes of fabrication tolerances, identified by their length scale:

1) Large scale variations (Figure 2) are larger than the circuit itself. A typical example of such a variation would be the layer thickness on a wafer. These tolerances will not affect a single circuit per se, but the fabrication yield on a wafer scale. For example, the layer thickness near the center of the wafer could match the layer thickness assumed in the design process and therefore circuits in that area would work properly. The layer thickness  $t$  gradually changes as the distance

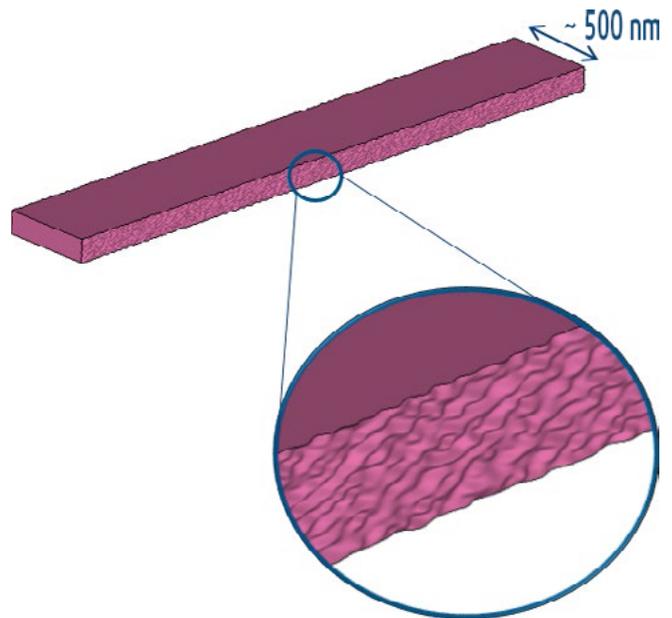
Circuit Geometrical Parameters	Corresponding Physical Parameters	Bandwidth	Ripple	FSR	Peak Frequency	Steepness
Si bridge width	Coupling coefficient of the outer X-couplers	□	□	x	x	■
Air gap width	Coupling coefficient of the inner X-couplers	■	■	x	x	x
Ring radius	Accumulated group delay in rings; attenuation (neglect $\ll 1$ )	□	x	■	x	x
Difference between lengths of the inner and outer rings	Additional phase shift between inner and outer rings	□	■	x	x	x
Correlated small variations of inner and outer rings radii	Similar phase shift introduced both to the inner and outer rings	x	x	x	■	x

**Figure 3:** Qualitative analysis of fabrication tolerances on overall circuit performance for certain design parameters.

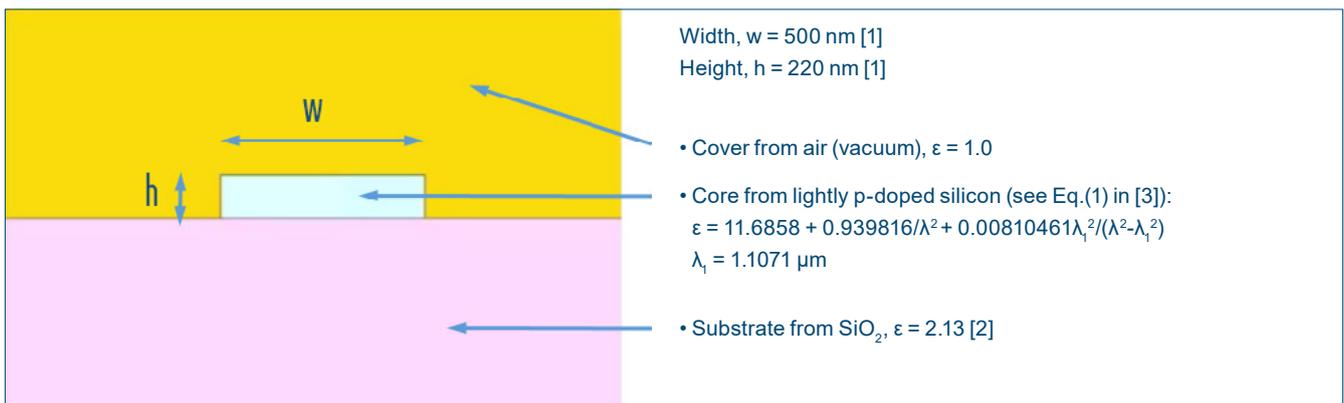
x weak/no dependence  
 □ moderate dependence  
 ■ strong dependence, crucial impact



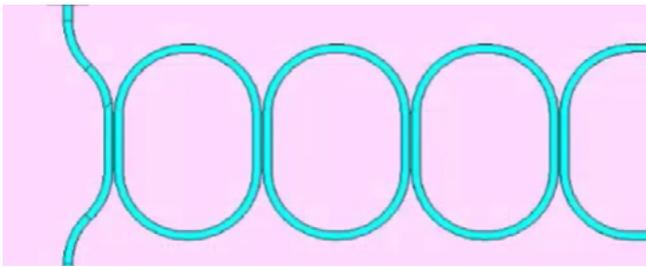
**Figure 4:** Medium scale fabrication variations.



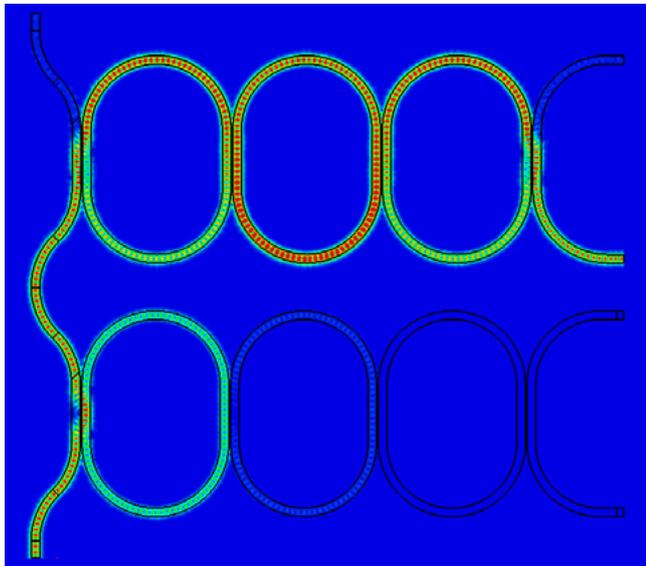
**Figure 5:** Small scale fabrication variations.



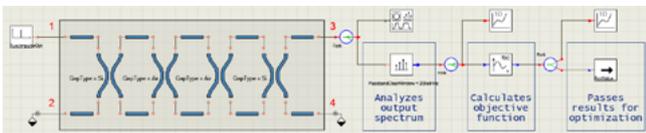
**Figure 6:** Cross section of the SOI waveguide.



**Figure 7:** Layout of a single filter.



**Figure 8:** Fields results calculated using CST Studio suite for a dual-band filter. The geometries of the two arms vary slightly such that light will pass through either the upper or the lower portion, depending upon the input wavelength.

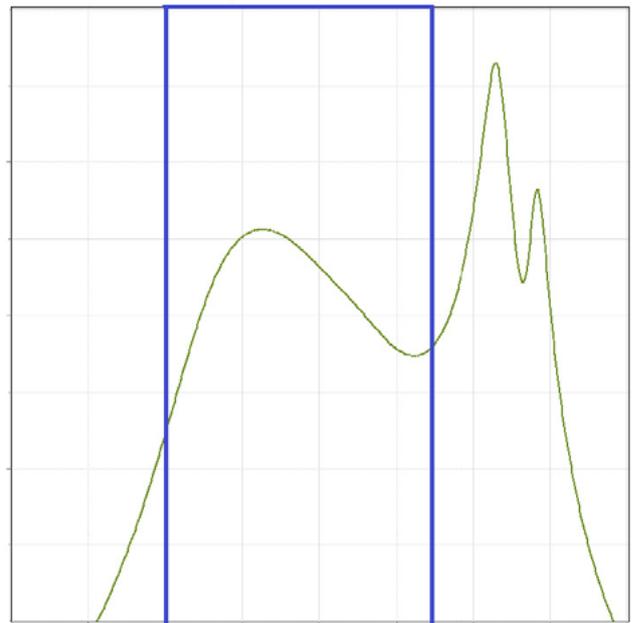


**Figure 9:** Schematic filter design in VPI Design Suite. The filter is represented by 4 couplers and connecting waveguides.

to the center increases. Eventually, the layer thickness has drifted too much and all circuits too far away from the center will fail. This effect can be corrected by making adjustments to circuits, depending on the position on the wafer.

2) Short range variations (Figure 5) occur on a length scale much smaller than the component size. A common example is the surface roughness of waveguide walls. It is a random variation, that can be averaged for each component. The effect of these variations can therefore be taken into account by using effective material properties.

3) Medium range variations (Figure 1) occur on the scale of the component size. A typical example would be the gap distance between two coupled waveguides. Variations on this scale are typically more random than the larger scale ones and they can affect the performance of any given component and the corresponding circuit independently from other circuits and components. It is necessary to make the circuit design itself robust against such variations.

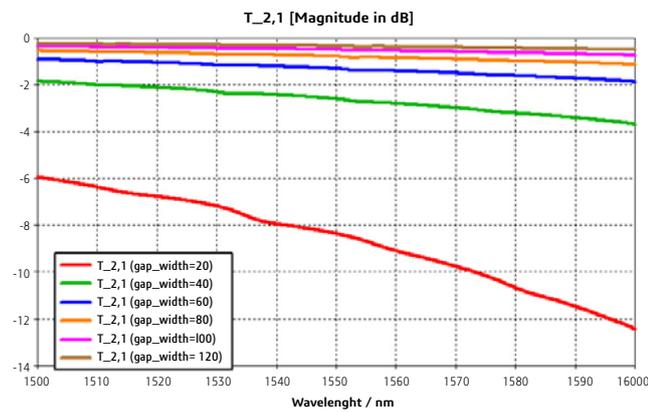


**Figure 10:** Initial transmittance of the filter (green) and desired filter response (blue).

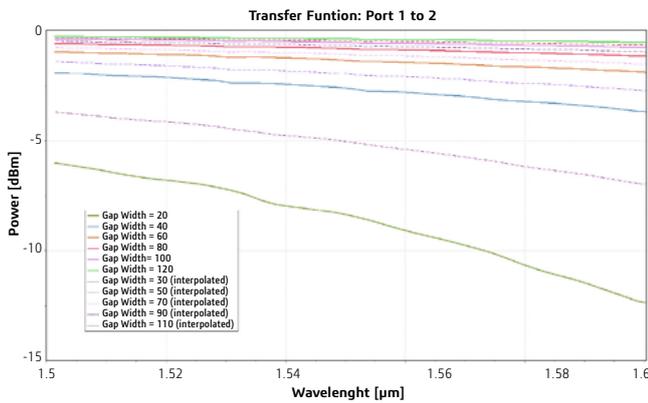
In this paper, we focus on variations on the medium scale, and how to make a circuit robust against them. The performance of a circuit is quantified by a figure of merit (FOM). For an ideal circuit, the task at hand is to simply maximize this FOM through optimization. With fabrication tolerances, the task becomes more difficult because the tolerances make it difficult to fabricate the circuit using exactly the optimal parameter combination and circuit performance might drop quickly as the parameter values start to deviate from the optimal combination. Accordingly, instead of shooting for the optimal parameter combination, the goal becomes to find a parameter combination that satisfies a minimum FOM threshold and is also sufficiently stable such that the FOM does not change too much when the parameters deviate from their target values. This process is generally referred to as a yield optimization and there are two possible approaches to it.

In the first approach, one defines the yield as a new figure of merit. This yield is calculated by assuming certain statistical distributions for each of the fabrication tolerances and then carrying out a Monte-Carlo (MC) analysis to determine the percentage of fabricated circuit samples that will still perform satisfactorily. The task at hand is then a direct optimization for the new FOM again, but each step of the optimization is computationally much more expensive.

The second approach is less rigorous but can be more efficient. Like for the ideal circuit, it is based on an optimization with respect to the original FOM. However, instead of optimizing the parameter values for the one global optimum, a number of local optimum values in the parameter space is calculated. The computationally expensive MC analysis described previously is not carried out for every step, but only for those local optimum values in order to identify that optimum which provides the highest yield.



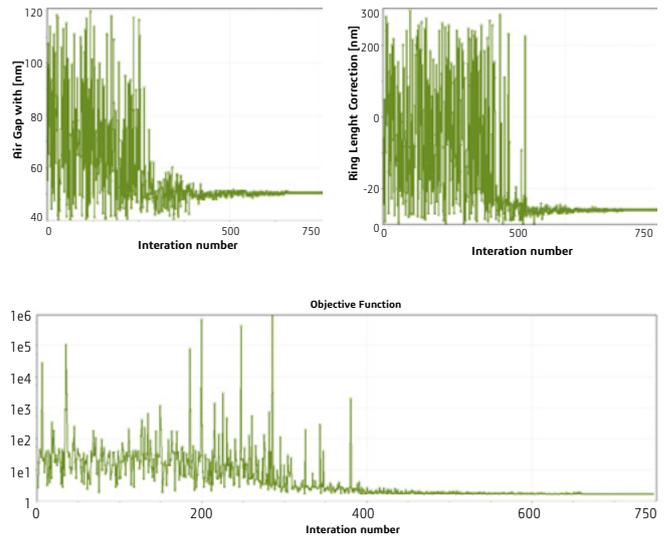
**Figure 11:** Transmittance of the air gap coupler for various gap widths, as calculated by CST Studio Suite.



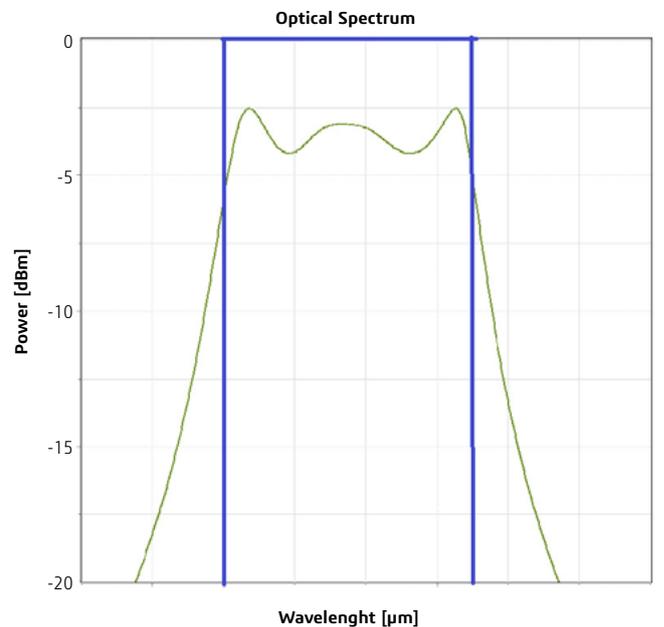
**Figure 12:** Transmittance of the coupler in VPI Design Suite as provided by CST Studio Suite, plus some interpolated curves in between.

For both approaches the number of parameters to include in the optimization can grow quickly, leading to a multi-dimensional optimization problem. Some of these parameters might not have a significant influence on the result, so their influence can be disregarded, thus keeping the dimensionality of the optimization at a reasonable level.

There are different approaches to the identification of the most relevant parameters. The best approach is generally to calculate the derivative of the figure of merit with respect to the investigated parameter. This derivative is a local quantity, so technically it needs to be evaluated for each step of the optimization, which adds significant time to the overall calculation. Accordingly, approximation techniques should be applied. For example, one can obtain an estimate of the derivative from interpolation between already calculated parameter combinations. This method will become more accurate as the optimization progresses and more samples are calculated. In this paper, we used a heuristic approach based on a qualitative analysis of only the first parameter combination.



**Figures 13, a-c:** Convergence of the objective function, along with the corresponding parameter values.

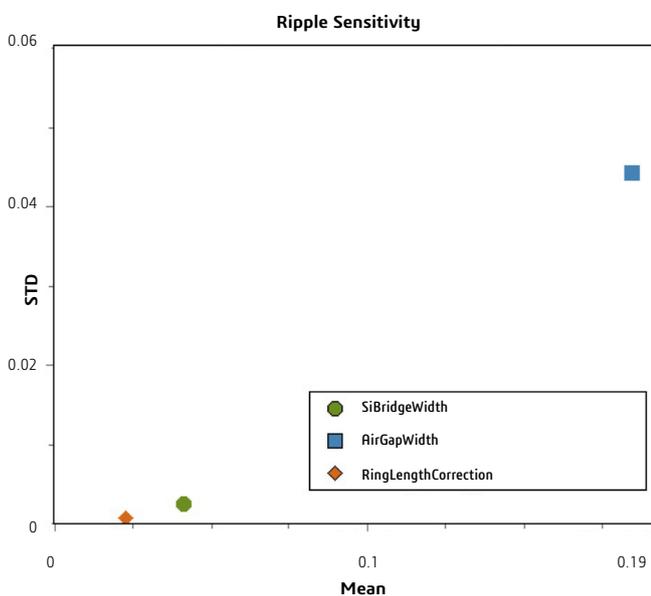
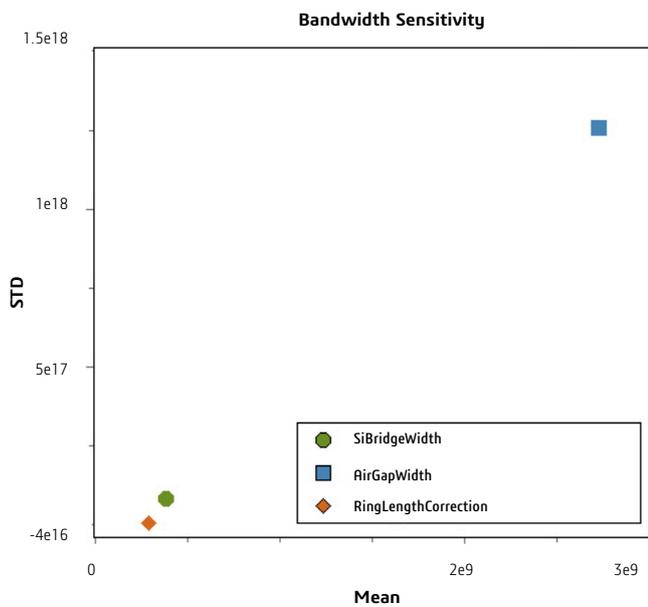


**Figure 14:** Optimized transmission spectrum of the filter (green) and desired filter response (blue).

## EXAMPLE USED HERE

The example used in this paper is based on [6]. It represents a bandpass filter that can, for example, be used in telecommunications applications. A silicon-on-insulator (SOI) technology is assumed, with the layer properties shown in Figure 6.

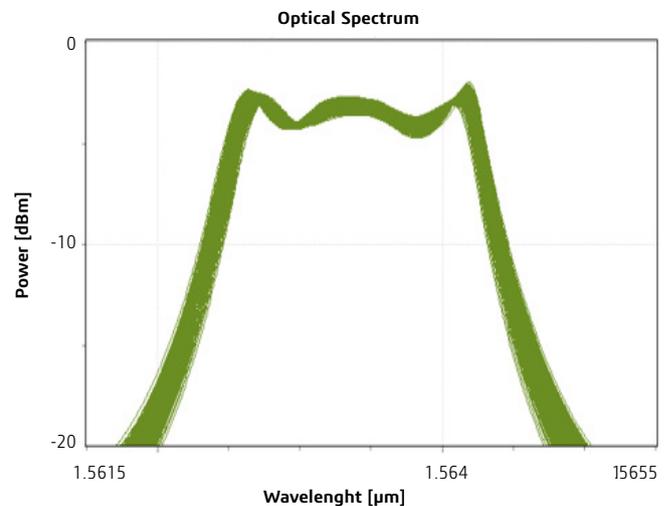
Assuming that each component in the PIC is coupled to other devices only via guided modes of optical waveguides (so-called “optical ports”) and coupling between evanescent modes of neighboring PIC devices could be neglected, one can segment the modeled PIC into individual building blocks. Further, the same components could be characterized with the same models, calculated only once. At the same time, the different devices in the same circuit could be modeled by different methods and with different accuracy. This allows for primary rapid prototyping of the circuit and detection of



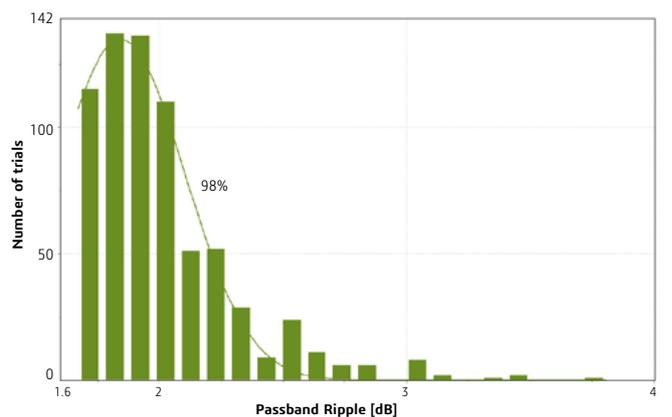
**Figure 15:** Influence of variations in air gap width, Si bridge width, and ring connector length on the overall filter performance.

the crucial components. This leads to improvement of the simulation accuracy for these identified components, which also decreases computation costs.

In the example used here, the filter is represented as two parallel waveguide coupler pairs connected by straight (in the first approximation) waveguides (Figures 7 and 8). The two inner couplers are evanescent couplers with an air gap between the waveguides. The two outer couplers are actually connected by an Si bridge, so that they are effectively Multimode Interference (MMI) couplers. For demonstration purposes, we use a simplified design process in this paper. It considers only the widths of the air gaps, as well as the added length between the inner couplers as parameters. The properties of the couplers are calculated from full-wave 3D simulations in CST Studio Suite and then used in an overall circuit simulation to calculate the complete filter behavior in VPI Design Suite (Figure 9).



**Figure 16:** a) Gaussian distribution of air gap width, and b) the corresponding changes in the transmission spectrum of the filter.



**Figure 17:** Histogram showing a 98% yield for the optimized circuit.

Figure X shows the initial transmittance of the filter, as calculated by the combined approach using VPI Design Suite and CST Studio Suite. Depending upon the desired accuracy and available hardware, this calculation can be carried out in a few hours, most of which is spent on the 3D simulation part. For reference, simulating the complete filter in 3D would take several days at high accuracy settings.

This performance advantage of the combined circuit/full-wave approach becomes even more pronounced when changing a parameter, e.g. the width of the airgap. If the parameter only affects one of the components, only this component needs to be re-calculated, whereas the full 3D model would need to be calculated in its entirety again. Interpolation between previously calculated parameter values can help to speed up the combined approach even further, and some parameters like the delay length between the couplers are solely defined on a circuit level.

## OPTIMIZATION

In order to optimize this design, we define the bandwidth and the flatness of the passband plateau as FOM:

$$\text{FOM} = (\text{Ripple in dB}) + (1 \text{ THz}) / ((\text{Bandwidth in THz}))$$

The properties of the couplers were pre-calculated for different parameter values.

Figure 11 shows the transmittance  $T_{2,1}$  of the air gap coupler for a varying gap width.

Figure 12 shows the transmittance from port 1 to port 2 after data conversion and import into VPI Design Suite, including some interpolated curves. It can be seen that the pre-calculated parameter calculations provide a rather good background for the interpolation, such that no further 3D simulations were used for the rest of the optimization.

Thus, after running a number of 3D simulations in advance to create the grid for interpolation, one can optimize the circuit performance rather efficiently. Figure 13 a–c show the corresponding convergence curves. The optimization begins to converge after about 400 steps and reaches the desired accuracy after about 750 steps (figure 14).

For this optimized circuit, we now study the influence of fabrication variations on the complete filter. A quick sensitivity analysis of all potential design parameters after the optimization confirms that fabrication variations in the air gap will have the strongest influence on the circuit performance (Figure 15).

Accordingly, we will focus on the air gap variation and assume a Gaussian distribution centered about the optimized value of 50 nm. The distribution and the corresponding changes in the transmittance are shown in figure 16 below.

Finally, as shown in figure 17, by plotting a histogram of the Monte-Carlo (MC) analysis, we find a yield of about 98%. While this might be sufficient for the simple circuit itself, a larger yield might be necessary if the circuit is part of a larger system where other circuits and their yields further reduce the overall system yield.

## SUMMARY AND OUTLOOK

In this paper, we discussed how circuit level and physical level simulations can be combined to optimize Photonic Integrated Circuits and how to balance accuracy and simulation speed. Efficiency can be further increased by using interpolation. This enables the engineer to study the effects of fabrication tolerances, and to calculate/optimize the expected fabrication yield.

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## AUTHORS

**Frank H. Scharf and Frank Demming**

Dassault Systèmes

**Eugene Sokolov**

VPIphotonics Inc

1 Edgewater Drive, Suite 108

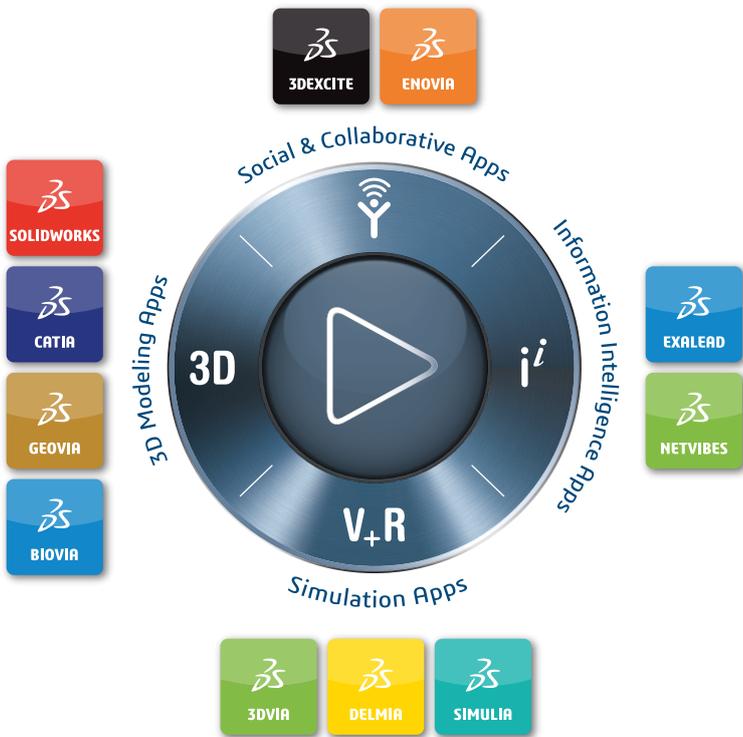
Norwood, MA 02062, United States

[eugene.sokolov@vpiphotonics.com](mailto:eugene.sokolov@vpiphotonics.com)

## CO-AUTHORS

**Sergei Mingaleev and Fyodor Morozko**

VPI Development Center



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**Asia-Pacific**

Dassault Systèmes K.K.  
ThinkPark Tower  
2-1-1 Osaki, Shinagawa-ku,  
Tokyo 141-6020  
Japan

**Americas**

Dassault Systèmes  
175 Wyman Street  
Waltham, Massachusetts  
02451-1223  
USA