Thermal - Fluid Co-Simulation of DNA Sequencing Thermocycler

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***Abstract**: Sequencing and amplification of DNA involves a precisely controlled thermal incubation cycle. Upscaling of traditional thermocyclers can be problematic due to non-uniformities induced across large incubation plates. Multiple chip profiles are studied to compare edge effects and promote uniform thermal histories across the incubation plate. Thermal performance is evaluated via steady-state heating within Abaqus/Standard. Transient cooling is modeled via Abaqus co-simulation by coupling thermal and fluid models.*

***Keywords**: Biomedics, CFD, Cooling, Coupled Analysis, Co-Simulation, DNA, Experimental Verification, Heat Transfer, Medical Device, Pipeline, Radiator, Thermal, Thermocylcler*

1. Introduction

Thermocyclers are commonly used to sequence and amplify deoxyribonucleic acid (DNA) arrays via incubation. A typical thermocycler assembly includes an incubation plate (thermal chip), heating element and means of cooling the chip. The chip contains an array of nodes which each hold a small volume (<1mL) of reagents to be cycled. The thermal chip discussed within this paper contains a rectangular array of three-hundred eighty-four nodes and incorporates a thin film electric heater mat, oil bath and network of internal pathways to circulate cooling fluid. Maintaining uniform thermal histories across the entire chip is critical to produce the necessary reactions at each node. However, achieving such uniformity over larger areas becomes problematic due to outer regions and corners of the chip having more potential for cooling whereas the inner region is inherently insulated by surrounding material. Figure 1 illustrates the thermal chip layout and nodal array.

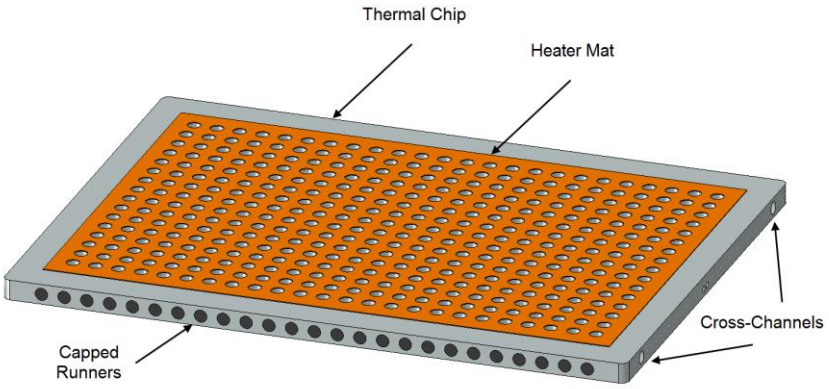

Figure 1. Thermal chip layout.

The thermal history of a node is primarily characterized by two factors: the steady-state thermal profile at elevated temperature and the amount of heat removed during the cooling process. This paper describes a method for modeling the chip's thermal history with successively more detailed simulations. Section 2 of this paper discusses the methodology used to create efficient and predictive models. Section 3 discusses the results of each model type and the subsequent design changes.

1.1 Description of Device

The device of interest consists of a metallic thermal chip with through-hole style nodes as opposed pocket-style wells. The chip is partially submerged in an oil bath which fills each node to the same liquid level. The oil bath is filled prior to operation and does not flow during incubation. The underside of the nominal chip configuration uses a single taper profile to prevent capturing air when filling. The electric heater mat affixed to the top surface of the chip is computer driven by a controller with feedback from a thermocouple located in the side of the chip. The heater mat is assumed to dissipate power evenly; characterized by a uniform isotropic body flux. During incubation, the top of the chip is covered with a temperature controlled lid which traps a finite volume of air above the nodal array. Figure 2 illustrates the nominal chip profile.

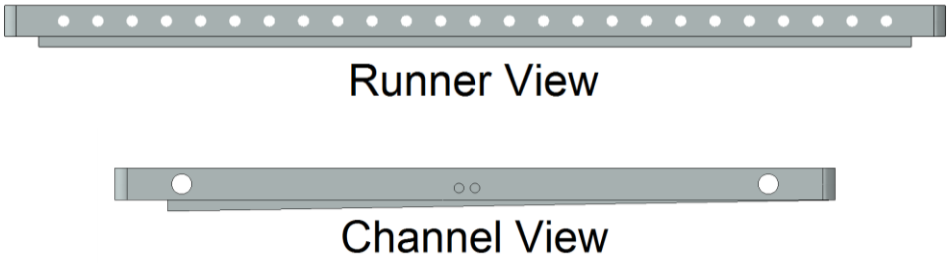

Figure 2. Profile of nominal chip with single slope taper.

The coolant path consists of two main cross-channels connected by twenty-five runners. The cross-channels flow along the first and last row of nodes whereas the runners flow alongside each column of nodes. The nominal configuration uses a single inlet-single outlet pattern with one fitting connected to each cross-channel on opposite corners of the chip. The nominal inlet is connected to the cross-channel over the thick side of the taper. The temperature and volumetric flow rate of incoming coolant are both known and can be controlled. Figure 3 illustrates the nominal coolant path.

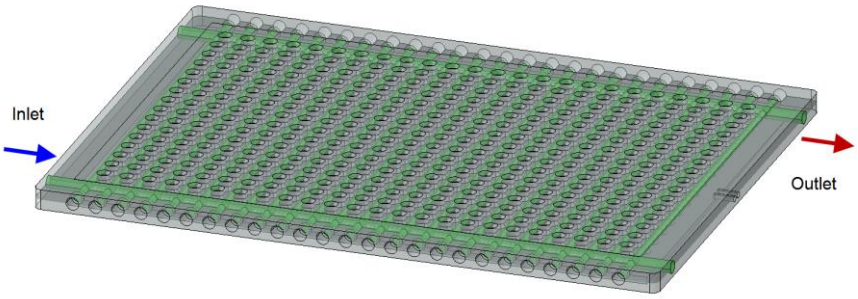

Figure 3. Coolant path of nominal chip.

1.2 Operation of Device

A single incubation cycling consists of three steps: temperature rise, steady-state hold at elevated temperature and coolant flushing to return to the initial temperature. The temperature rise and hold steps are driven by the heater mat's power dissipation with coolant present but not flowing. At the end of the elevated temperature hold, the device can be assumed to have reached a thermal steady-state condition. In the flushing step, coolant flows via constant displacement pump with no power dissipated from the heater mat. Inlet coolant is considered to have a constant temperature and flow rate. Outlet coolant is circulated through an external circuit which returns it to the pump at the prescribed inlet temperature. Nodal and coolant temperatures are on the order of 50°C to 100°C.

1.3 Problem Description

The nominal design produced diminishing results in nodes farther from the center of the chip. Inadequate reactions were observed toward the corners of the array and most notably near the coolant inlet. Thermal video of the device indicated the outer most regions were of lower steady-state temperature and tended to cool faster than the central region. Figure 4 shows two temperature plots scaled from room temperature (blue) to the set point (red); one taken at steady-state and another during flushing. These observations led to the hypothesis that low nodal temperatures and overexposure to coolant flow caused the incomplete reactions. Thus, revisions to chip geometry and configuration of fluid flow are presented to improve device performance.

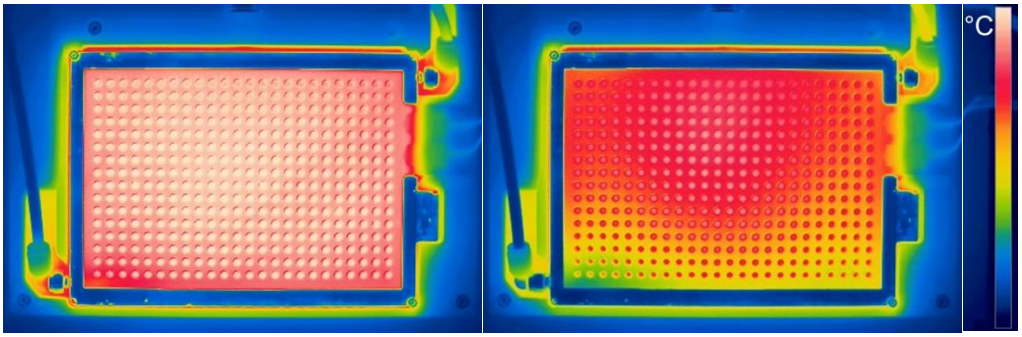

Figure 4. Thermal images of nominal configuration: Steady-state (left) and flushing (right).

2. Methodology

Refined models of the device were created based on known operating conditions and limitations of the physical design space. While fluid models include only the coolant path, thermal models include the chip, housing, oil bath, and air above the chip. Justification for selecting this control volume is supported by thermal video of the device in operation. The elevated thermals of the chip are seen to be primarily contained within the oil bath and insulated by the surrounding housing. The height of air above the chip represents the ceiling height of the lid. Since the lid can be thermally controlled via its own electric heater plate, the top surface of the air is defined as a temperature boundary condition. A temperature boundary condition is also applied to the bottom surface of the assembly such that the underside of the oil bath is considered to be a thermal sink. All vertical surfaces of the assembly are prescribed zero heat flux. Modeling of boundary conditions in this way provides a consistent means of comparing temperature gradients across the nodal array. Figure 5 shows the assembled thermal model and applied boundary conditions. The effects of thermal radiation and free convection are absorbed by the top and bottom surface boundary conditions. All heat transfer within the control volume is assumed to be perfect thermal conduction with zero contact resistance. Thermal strains are considered negligible for the purpose of this model and are not included.

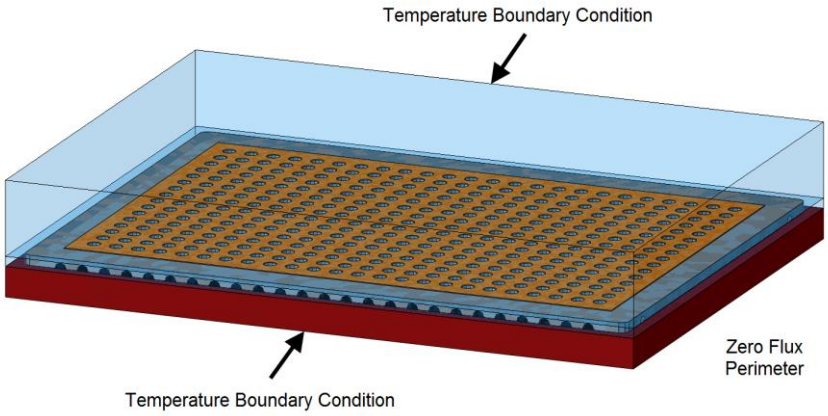

Figure 5. Model assembly and boundary conditions.

2.1 Modeling Methods

Three modeling methods are used to evaluate each design's potential for improving uniformity of nodal thermal history: steady-state thermal, transient fluid and co-simulation of transient thermal coupled with transient fluid. Changes to the chip geometry are first evaluated with a steady-state thermal model. Flow pattern changes are also first evaluated using a stand-alone model. Before coupling new designs via co-simulation, results from both models are compared with respect to temperature distribution and local flow velocities. Comparing results in this manner helps to assess each combination's potential for increasing the uniformity of nodal thermal histories.

The aforementioned surface temperature boundary conditions and heater mat body flux were calibrated by tuning a steady-state model of the nominal configuration to experimental temperature probes and thermal imaging results. Calibration of steady-state heater mat power dissipation was repeated for each new chip profile such that the model represents the device at its temperature set point. Stand-alone fluid models were created to study flow patterns without thermal considerations. Due to manufacturing constraints, revisions to the fluid path were primarily focused on the number and location of inlet/outlet points. The nominal configuration was compared to multiple design iterations which split the inlet and outlet flow volume amongst the cross-channels and runners. All flow conditions are defined by a constant inlet velocity, based on a mass flow rate, with a zero pressure boundary condition at each eligible outlet. Only laminar coolant flow is considered.

Co-simulation models were created to simulate coolant flushing after the chip has reached an elevated temperature. These models are comprised of two steps: an initial steady-state thermal analysis without fluid flow and a transient thermal analysis coupled with transient fluid flow. The boundary conditions are identical to the respective stand-alone models with the addition of thermal properties being applied to the fluid. In the first step, the device (less coolant volume) is powered

to the temperature set point. At the same time, the outer surface of the coolant volume is also prescribed with the same set point temperature. In the second step, the heater mat is turned off and the inlet coolant begins to flow with a constant temperature at constant velocity.

3. Results and Discussion

3.1 Nominal Configuration

Steady-state thermal and fluid flow results agree with experimental observations of the nominal chip. Regions of inadequate performance were found to have lower than average chip temperature and strong potential for undershoot during flushing. Figure 6 compares steady-state chip temperature with coolant velocity. Both plots are individually scaled from low (blue) to high (red). Temperature is scaled over a two degree range; +/- 1°C about the set point. Coolant velocity is scaled from zero to an undisclosed threshold value. Velocity regions which exceed this limit are plotted using the same color as the threshold. The chip is shown to have a central thermal epicenter that is shifted toward the thin side of the single slope taper. The flow analysis shows several runners with low flow rate in the same region. Conversely, runners of high flow rate are located along the perimeter and in regions of low nodal temperature. Note that fluid flow plots are shown as a cross-section through the center of the pathway.

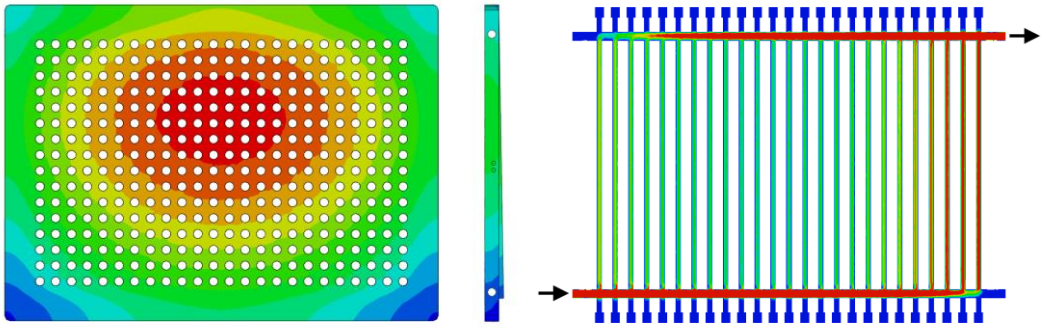

Figure 6. Nominal configuration: Steady-state chip temperature (left) and coolant velocity (right).

Co-simulation results confirm the combined effect of having high flow rate paired with low initial temperature. Moving more coolant through these regions exacerbates incomplete reactions by causing thermal undershoot during flushing. Figure 7 compares three temperature plots while flushing coolant: a thermal image of the experiment, co-simulation of the chip and co-simulation

of the coolant. The thermal image is scaled from room temperature (blue) to the set point (red). The co-simulation results are both scaled in a similar fashion over a range of fifteen degrees Celsius, with the upper limit defined as the set point. The objective of subsequent revisions is to create a more uniform temperature distribution paired with runner flow rates proportional to the thermal gradient. The culmination of nominal configuration results supports leveraging stand-alone models prior to coupling different physics. For this particular application, uncoupled models can be used separately to more quickly understand a configuration's initial temperature distribution and potential for uniform cooling.

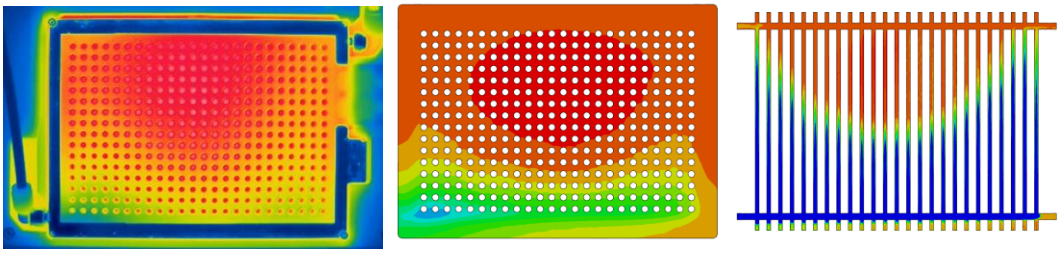

Figure 7. Flushing temperature of nominal configuration: Thermal image (left), co-simulation chip (center), co-simulation coolant (right).

3.2 Revised Configuration

Several design revisions were inspired by the nominal results. The most promising configuration modifies the underside of the chip to a double slope taper as shown in Figure 8. The intention of the double slope is to raise the nodal temperature along the perimeter while adding thermal mass to the inherently insulated center region.

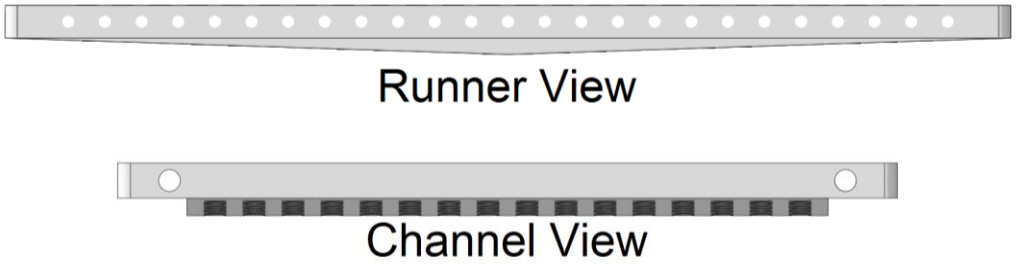

Figure 8. Profile of revised chip with double slope taper.

Revised coolant conditions redefine the inlet temperature to be more near the set point and enter at a higher flow rate. These revisions reduce the coolant versus chip temperature difference and increase the coolant volume circulated by a factor greater than two, respectively. Both cross-channels were moved outward, away from the nodal array. Two coolant inlets and two outlets were symmetrically positioned about the middle runner on adjacent sides of the chip. Figure 9 illustrates the revised coolant path.

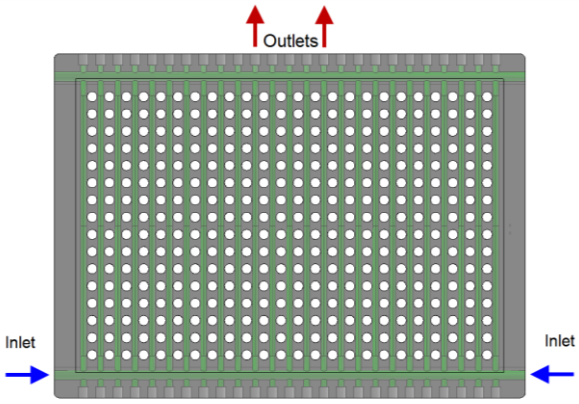

Figure 9. Coolant path of revised chip.

The stand-alone models suggest a double slope taper will more evenly distribute power from the heater mat and more uniformly cool the chip. Figure 10 shows steady-state chip temperature and coolant velocity scaled to the same values as Figure 6. The revised configuration produces half the temperature gradient across the chip and the symmetric fluid path more evenly distributes flow amongst the central runners.

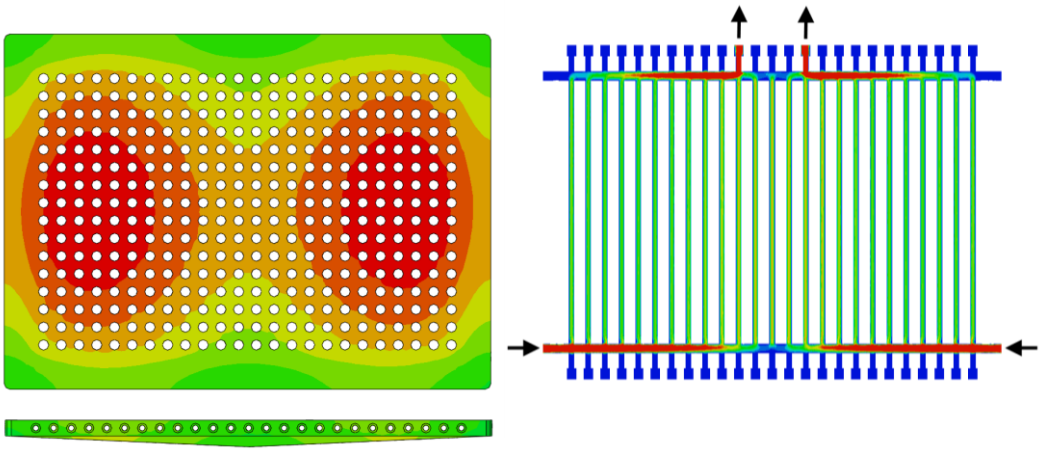

Figure 10. Revised configuration: Steady-state chip temperature (left) and coolant velocity (right).

Co-simulation confirmed a more uniform thermal history is achieved by symmetrically dividing the flow and using a higher coolant temperature with a higher flow rate. Figure 11 illustrates this improvement. The plots shown are taken at the same time point and scaled to the same temperature range as Figure 7. The revised configuration has a more evenly distributed flow front which, when combined with the double slope taper, produces a more uniform temperature gradient during flushing. Moving the cross-channels outward, away from the nodal array, also reduces the potential for thermal undershoot of nodes near the corners and inlets.

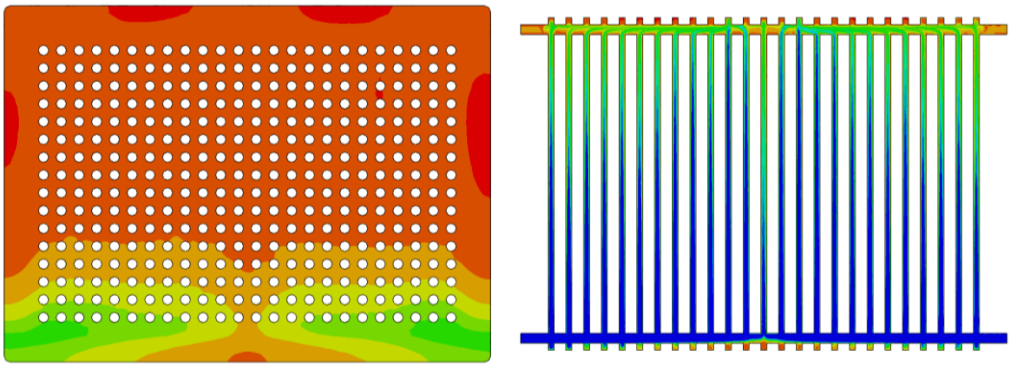

Figure 11. Flushing temperature of revised configuration: Co-simulation chip (left) and coolant (right).