Predicting post-drop failure of ceramic chip capacitors using Abaqus/Explicit

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***Abstract**: C-chip capacitors are known to undergo flex cracking during passive bending tests, and would undergo burnout when current passes through it. In general post-impact functional test is considered to be sufficient to establish if a system can withstand a set of drops as prescribed by the standards. A case of capacitor burn-out during post-impact functional test has been taken up for the current study. With an objective of understanding the system dynamics and the mechanics of failure, explicit dynamic simulations were done. Simulations could predict existence of strain peaks possibly exceeding the failure limits considered and existence of displacement hinges post-drop. The orientation of the c-chip was altered taking hints from the simulation. Further testing did not produce any system failure in post-impact functional tests. The paper discusses the methodology adopted in the current study and its limitations from the perspective of predicting failure.*

***Keywords**: Drop impact, Flex crack, Ceramic chip capacitor, Component orientation.*

1. Introduction

Accidental drop may occur in the assembly line and transients generated by drop can sometimes be severe enough to cause failure of components. Failure of relatively large SMD or PTH components can be easily detected. Electronic devices make use of several small ceramic chip capacitors and resistors (c-chips) mostly of the order of a few millimeters in dimension. Unlike the big components, solder failure and component separation are less common with c-chips. Most of the times we have to rely on functional tests to establish reliability of these components. System failure is taken as an identifier of possible component failures, and becomes a trigger for further investigations.

C-chip failure by crack formation through the component is a known mode of failure when subjected to flexure, and has been discussed in several studies **[1-2]**. Quasi-static bending tests subjecting the c-chips to pure bending have been used to quantify such failure in terms of the PCB displacement or strain. Since the strain limits are generally established by quasi-static tests, there is a scarcity of dynamic failure data for such components. Numerical simulations make use of similar limits to understand the reliability of c-chips in the virtual world as simulations explicitly modeling these c-chips are computationally very expensive. Moreover, both constitutive behavior and failure model characterization of the dielectric-metal layer composite structure is difficult at the user's end, and not much of published data is available. Measurement of strains developed in the c-chip is also not reported.

In the current study, the failure of a c-chip capacitor in an automotive control unit is discussed and the capability of drop simulations performed using Abaqus/Explicit to predict the reliability of c-chips is inquired. The ability to simulate the PCB dynamics and the distribution of strain is made use of in order to make decisions on component orientation changes. The deviations observed in further re-validation and possible causes for the same have also been discussed.

2. Experimental details and observation

Drop tests are performed on a simple free-fall test setup. The DUT is mounted on to an extended arm held with an electromagnet. When released the assembly falls under gravity and allows the DUT to hit the floor at a desired drop orientation. In the particular case the electronic package after a successful pre-drop functional test is subject to free-fall along the thickness direction of the PCB from a height of 1m.

2.1 Observations during post-impact functional test

The ceramic chip capacitor under consideration (figure 1) is aligned along the transverse direction of the PCB. The location of the capacitor is adjacent to the cooling bank and PCB flexing can occur about this region.

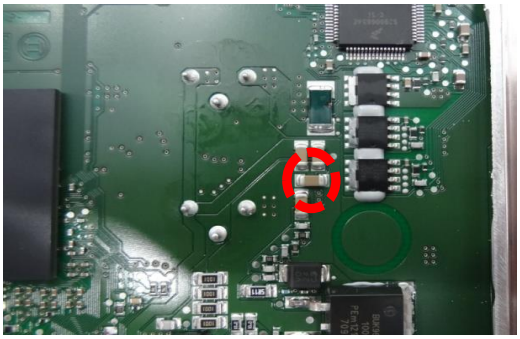


Fig 1. Ceramic chip under consideration (undamaged state)

Post drop, the electronic packaging is subjected to a functional test wherein the components are subjected to a designed electrical load. This is done as a procedure to primarily ensure that there are no discontinuities generated as a part of the test. The droped DUT failed in the functional test and a further examination after disintegration of the housing revealed capacitor burnout (figure 2).

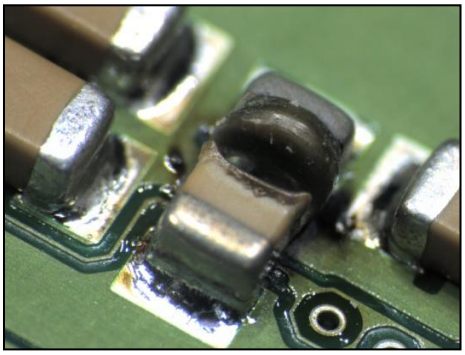


Fig 2. C-chip burnout during post-drop functional test

2.2 Flex crack

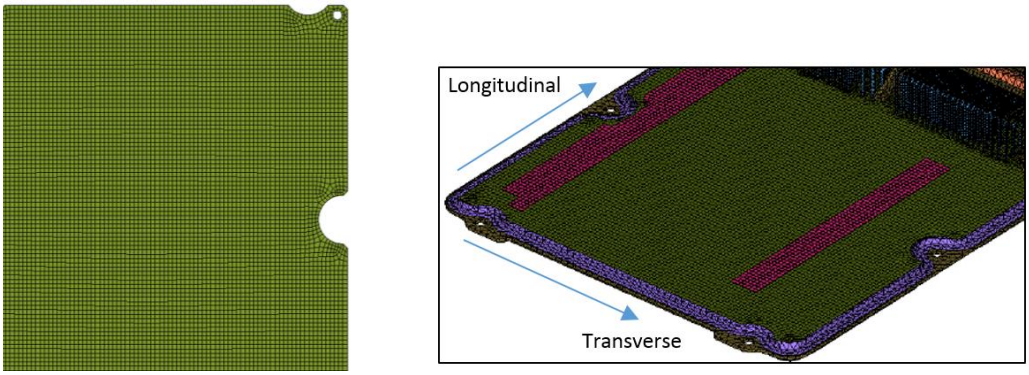
One of the most important causes of capacitor burnout is flexure induced cracking, generally termed as flex crack. The ceramic chips have a layered construction of ceramic material and thin metal coatings to provide the required capacitance/resistance. Ceramic materials being brittle, the c-chips are vulnerable to damage when bent about the soldered ends. Cracks form when the PCB strains along the length of the capacitor near the solder region exceeds certain limits decided by several factors including the size of the chip. This causes a jump in the capacitance/resistance value and renders the chip unusable impairing the functionality of the device.

3. Simulation methodology

3.1 Finite element model and simulation strategy

A finite element model of the assembly was made using Hypermesh to optimize the total degrees of freedom with appropriate mesh quality requirements. Hex dominated mesh with 46230 elements and 63572 nodes, and 3 elements across thickness were used. C3D8I elements were employed in areas of interest away from pin/connector. The mesh

details of the PCB and the axes definitions have been shown in figure 3. Node number 506464 has been used to represent the ceramic chip capacitor under investigation (figure 4). Orthotropic material properties as mentioned in table 1 were employed to model the PCB. No attempt at using homogenized data was made in the current study.



(a) (b)

Fig 3. (a) Mesh details of the PCB (b) Details of axes definitions

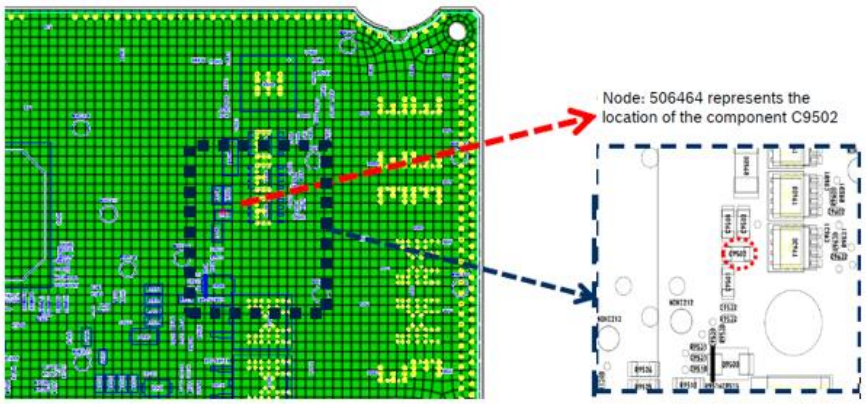


Fig 4. Node identified to represent the capacitor

Table 1: Orthotropic elastic properties assumed for the PCB material

Ex	Ey	Ez	PR-xy	PR-xz	PR-yz	Gxy	Gxz	Gyz
MPa	MPa	MPa				MPa	MPa	MPa
17850	17850	7055	0.15	0.35	0.35	6611	6611	7760

Numerical simulation of the drop event was performed using Abaqus/Explicit. Explicit procedure saves a lot of effort in addressing convergence and associated stability issues. For complex assemblies this method also has an advantage of defining frictional interaction between the parts through general contact definitions and capturing the contribution of rebound more realistically. Nevertheless for a first-cut simplified predictive model, a mode-based procedure could be a substitute approach which however is not the focus of the current study.

Drop from a height of 1m was simulated by defining the initial velocity of the body, obtained by assuming loss-less conversion of the initial potential energy of the body into its kinetic energy. Acceleration due to gravity was defined while any possible resistance from air was neglected. The details of the drop configuration and the initial parameters

defined are shown in figure 5. The impact surface was modeled as a perfectly rigid flat shell. The events from initial drop to a period of 4ms were studied. General contact with a frictional coefficient of 0.2 was employed in the study.

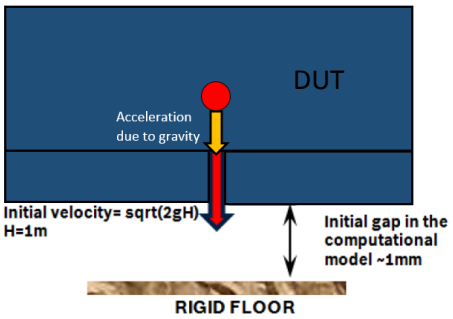


Fig 5. Drop configuration and initial parameters defined in the computational model

4. Results and Discussion

4.1 Simulation results

The contour of the strain on the PCB is shown in figure 6. For the current study, a strain limit of 1200 micron strain was adopted. There is a clear indication that the PCB strains at the capacitor location exceeds the safe limits indicating that the solder region experiences considerable strains. The time history plot of strain (figure 7) indicates that compressive strain starts building up in the PCB and there is a reversal until the tensile strains reach a peak after which the next cycle initiates. The result clearly shows that the peak strain exceeds the safe limits by approximately 5.5 times and persists for almost a millisecond, with reversals beyond the assumed safe range.

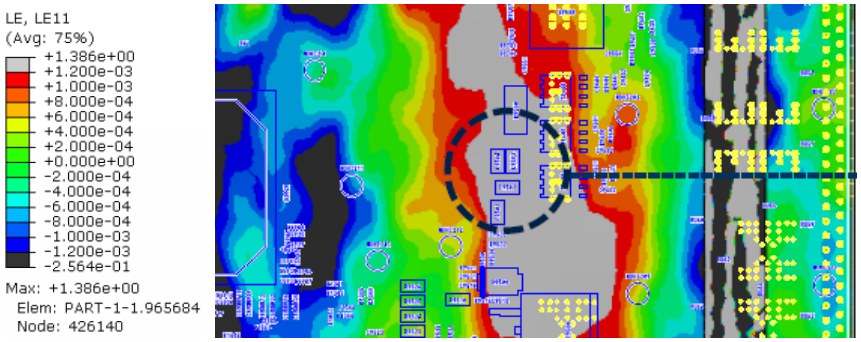


Fig 6. Strain distribution on the PCB in the vicinity of failed C-Chip (overlaid image):

Increment 206156: Step Time = 2.88 e-3 s

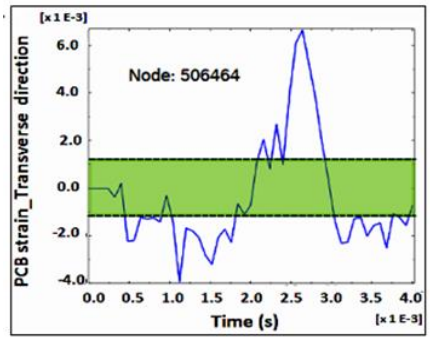


Fig 7. Temporal variation of strain at the cchip location

It was now necessary to understand the flexural behavior of the PCB to determine its contribution to component damage initiation. Transverse and longitudinal sections passing though the node representing the capacitor location were extracted at various step times. The nature of PCB displacement was analyzed to obtain any hints on the effect of it on component failure.

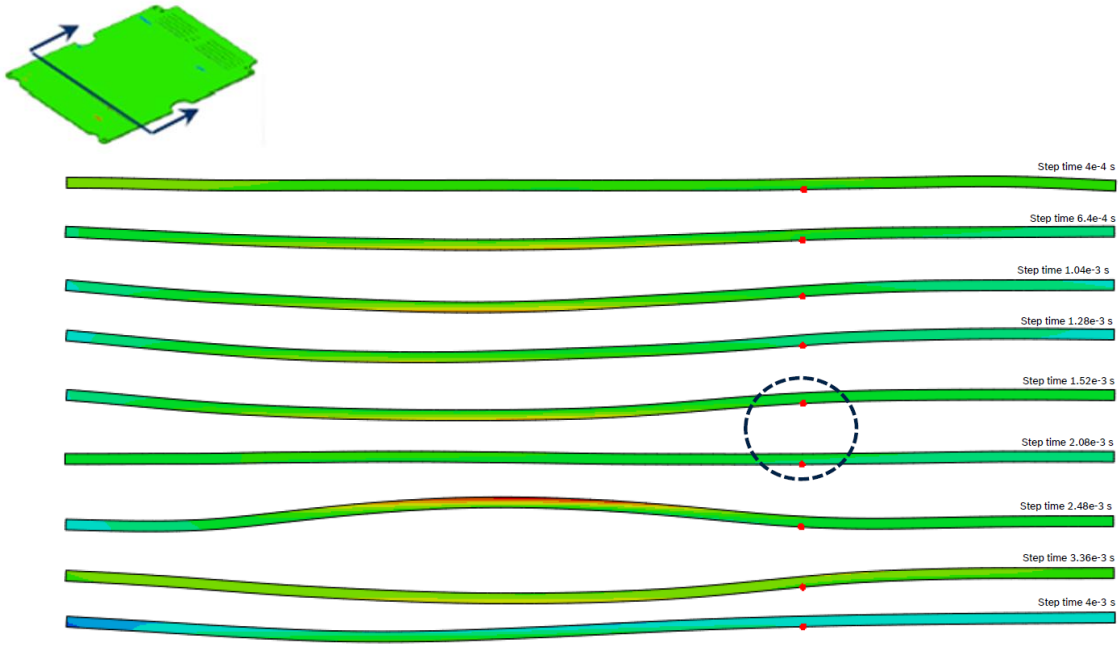


Fig 8. Transverse section of the PCB

Transverse section (figure 8) shows PCB bending and hinge effect near the component location. There is a gradual motion of the hinge away from the capacitor location followed by reversal of the curvature as the time progresses, indicating that the component has been placed in a location conducive to damage initiation. This appears to be in contrast with the component supplier's recommendation that the chip be located horizontal to the direction in which stress acts (figure 9).

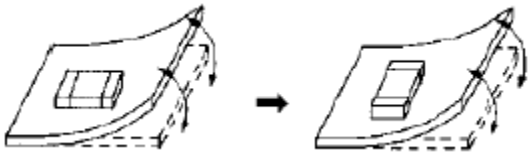


Fig 9. Supplier recommendation on the mounting of c-chip capacitor

(Figure Courtesy: Murata Product specification for approval **[3]**)

An examination of the longitudinal sections reveal that there is almost no motion of PCB at the mounting location of the neighbouring capacitors as highlighted in figure 10. This explains why the other two capacitors did not undergo any damage during drop. The result also indicates that the capacitor can be re-oriented along the longitudinal direction to prevent damage. A careful observation again shows a possible hinge location very near to the capacitor location of interest. This was however neglected in the first instance and a decision on re-orienting the component was made. The altered layout is shown in figure 11.

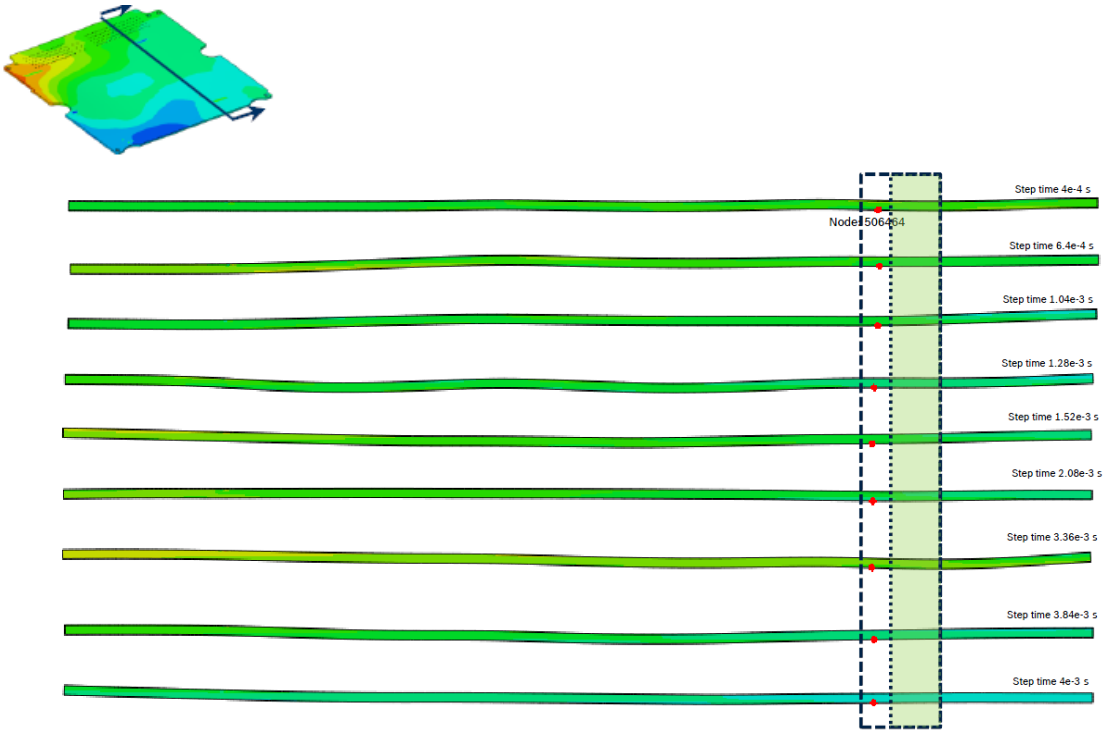


Fig 10. Longitudinal section of the PCB

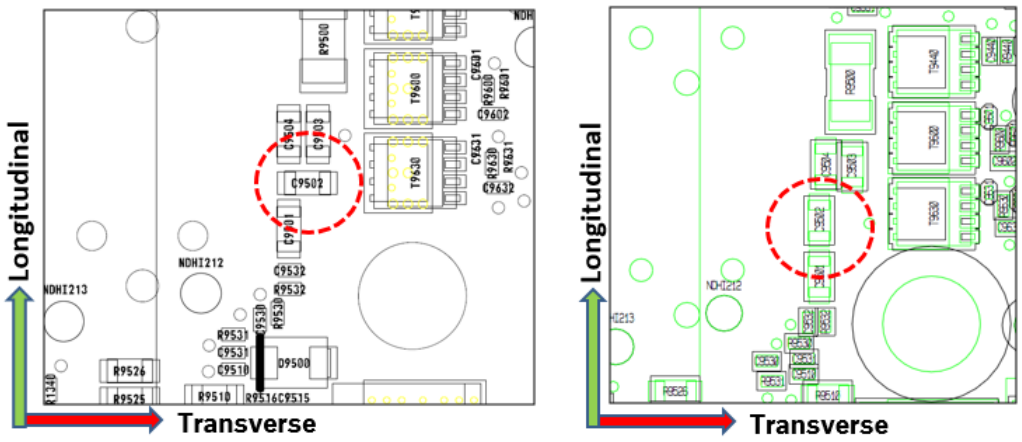


Fig 11. New layout decided based on the simulation results (old layout is included for reference)

4.2 Experimental revalidation and comments

The DUT with revised layout was dropped under similar specifications. The device passed the post-impact functional test. In order to confirm the absence of damage in the c-chip, cross-sectional analysis was done. The cross-section showed partial crack on the component. The flex crack is shown in figure 12. Similar findings in quasi-static bending tests have been reported earlier.

Fig 12. Partial flex crack revealed through cross-sectioning

It may be unfair to undermine the predictive capability of the tool considering that the flexibility in extracting multi-step results and capability of visualization was indeed helpful in understanding the behavior of PCB. The effect of assumptions on the material properties employed, neglected hinge on the proposed location and the adopted strain limit itself add to the uncertainties in predictability of the model. Contribution of component removal method for cross-sectioning itself should be thought about **[4]**. A study using sub-models should aid us in appreciating the strains developed on the component. However as discussed earlier, a suitable material representation scheme has to be identified for such simulations for any benefit. In the presence of such uncertainties, the usage of Abaqus/Explicit for predicting drop generated c-chip failure using the discussed methodology is justifiable and quite beneficial for efficient product development.

5. Summary

Drop simulation using Abaqus/Explicit was performed to understand the PCB deflection and strain developed in the vicinity of the capacitor location. The tool is capable of simulating the dynamics of the PCB very well. The indications of the results were used in reconsidering the existing layout. A review of the uncertainties introduced by the assumptions made and examination of the effect of inclusion of certain neglected observations from the simulation results could make the model more robust. Efforts are being made to improve the predictability of the model through sub-modeling capability of Abaqus with additional investigations into material characterization.

6. References

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[3] Murata Product specification for approval, Spec No. JEMCG2-10342A, Issued on 27 Aug 2004

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